Abstract of the Disclosure

A multiplierless IIR filter incorporates power-of-two coefficients to perform shift operations to reduce space and increase speed. To optimize performance, a genetic algorithm generates the power-of-two coefficients. The filter architecture includes shift registers to receive input samples and previous outputs. A shifter stage is employed to perform shift operations for the input samples and previous outputs based on corresponding power-of-two coefficients. Products are added by parallelism and sequential pipelining to produce an output.